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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,928	03/31/2001	John T. Orchard	15685P096	7550
43831	7590	02/14/2006	EXAMINER	
BERKELEY LAW & TECHNOLOGY GROUP			NGO, CHUONG D	
1700NW 167TH PLACE			ART UNIT	
SUITE 240			PAPER NUMBER	
BEAVERTON, OR 97006			2193	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

09/823,928

Applicant(s)

ORCHARD, JOHN T.

Examiner

Chuong D. Ngo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09/22/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2,4-17 and 19-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2,4-17 and 19-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 2,4-17, and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (6,535,901).

As per claims 2,11,12,14-17,26,27 and 29-31, Grisamore discloses in figures 5 a method for implementing a Wallace-architecture in which input terms are analyzed on a bit-wise basis (see the bridging paragraph of cols. 4 and 5, where each level of bit significance is a column of bit) to segment each level of bit significance of input terms into one or more-groups of three bits (circled three dots), and/or one or more groups of two bits (circled two dot and/or one or more group of one bit (non-circled dots). Full-adders (3-dot circle) and half adders (2-dot circle) are selected to perform Boolean functions on 3-bit groups and 2-bit groups, respectively. The number of adders are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance as claimed (see the bridging paragraph of cols. 4 and 5). It is noted that Grisamore does not teach registers in figure 5. However, Grisamore discloses in col.1, lines 33-40 that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit. Thus it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Grisamore with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

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2. Claims 2,4-17 and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Costa et al. (5,935,201).

As per claims 2,11,12,14-17,26,27 and 29-31, Costa et al. discloses in figures 7-9 a Wallace-architecture in which full-adders (3-input block) and half adders (2-input block) are selected to perform Boolean functions respectively on 3-bit groups and 2-bit groups in each level of bit significance of input terms (each adder in figures 7 and 8 is labeled corresponding to the levels of bit significance of input terms) . The numbers of adders are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. Groups of one bit are corresponding to the input terms that are not input to an adder in figures 7 and 8 . It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit, it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Costa et al. with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

3. Applicant's arguments filed on 10/26/2005 have been fully considered but they are not persuasive.

Regarding registers for receiving one-bit group, it is respectfully submitted that to implement the multiplication in figure 5 of Grisamore, for example, in a pipelined fashion, an

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upper layer (the top layer #6, e.g.,) should provide all the signals to a lower layer (the next lower layer #4, e.g.) at the same time. Therefore, the need of registers to hold those bit (1-bit groups) that are not processed by either full or half adder in the top level 6 is obvious in order to wait for the full and half adders to process 3- and 2-bit groups.

Regarding bit-wise analysis, it is respectfully submitted that Grisamore clearly discloses in the bridging paragraph of cols. 4 and 5 the selections of full and half adders based on a bit-wise analysis of the input terms within each level of bit-significance as columns of bits. Further, in both figure 5 of Grisamore and figure 8 of Costa, full-adders (FAs) and half adders (HAs) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. For instance, in figure 5 of Grisamore the number of full-adders and half adders in each column (level of bit-significance) is not arbitrary, but are differently selected for each column depend on the number of product terms in that column. For example in figure 5 of Grisamore, there is a HA in column 1 having three product terms, a HA and a FA in column 2 having four product terms, and a HA and two FAs in column 3 having 5 product terms, etc. Changing the number of product terms in a column would clearly change the numbers of FA and HA in that column.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The reference to Yamazaki et al. (4,706,211) is cited to show an example of pipelined circuit.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong D Ngo
Primary Examiner
Art Unit 2193

02/06/2006